

# Laboratory 2

(Due date : **002/003**: October 7<sup>th</sup>, **004**: October 8<sup>th</sup>, **005**: October 9<sup>th</sup>)

## OBJECTIVES

- ✓ Use the Structural Description on VHDL.
- ✓ Test arithmetic circuits on an FPGA.

## VHDL CODING

- ✓ Refer to the [Tutorial: VHDL for FPGAs](#) for a list of examples.

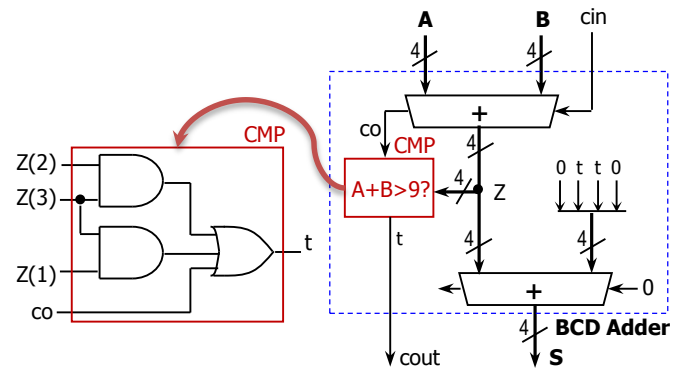
## FIRST ACTIVITY (100/100)

- **PROBLEM:** BCD Addition of two numbers. The operands ( $A$  and  $B$ ) are 4-bit numbers represented in BCD (where only numbers from 0 to 9 are allowed). The result  $S$  is also represented in BCD. There is also a BCD carry out ( $cout$ ). If any of the operands is greater than 9, the result  $S$  is invalid.

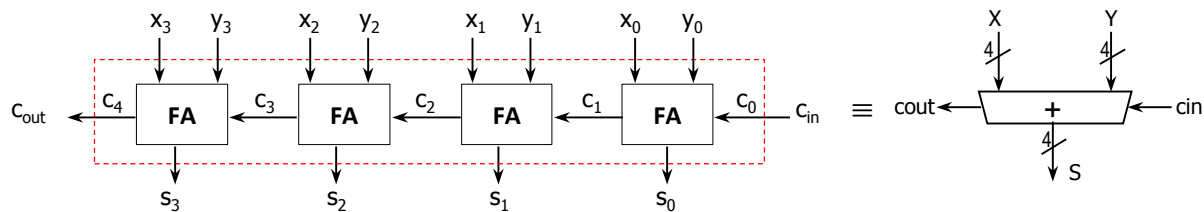
Example:  $7 + 8 = 15$ . Here,  $cout = 1$ , and  $S = 0101 = 5$ .

This circuit can be built out of two 4-bit binary adders and a few logic gates as depicted in the figure  $\Rightarrow$

- ✓ Operation: If  $A + B > 9 \rightarrow S = 6 + Z$ ,  $cout = 1$ . Here, by adding 6, we "correct" the binary sum to make it look as BCD code. If  $A + B \leq 9 \rightarrow S = Z$ ,  $cout = 0$ .

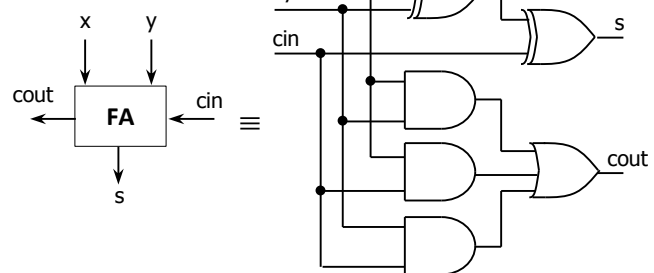


- The figure below depicts the internal architecture of the 4-bit binary adder. The full adder circuit is also shown.



- ✓ **NEXYS A7-50T:** Create a new Vivado Project. Select the **XC7A50T-1CSG324 Artix-7 FPGA** device.
- ✓ Write the VHDL code for the BCD Adder. Use the Structural Description: Create a separate file for the Full Adder, the 4-bit adder, the 'CMP' block, and the top file (BCD Adder).
- ✓ Write the VHDL testbench to test the circuit for the following cases:
  - ♦  $A=0x6$ ,  $B=0x4$ ,  $cin=0 \rightarrow cout=1$ ,  $S=0000$
  - ♦  $A=0x8$ ,  $B=0x9$ ,  $cin=0 \rightarrow cout=1$ ,  $S=0111$
  - ♦  $A=0x4$ ,  $B=0x8$ ,  $cin=1 \rightarrow cout=1$ ,  $S=0011$
  - ♦  $A=0x5$ ,  $B=0x8$ ,  $cin=1 \rightarrow cout=1$ ,  $S=0100$
  - ♦  $A=0x2$ ,  $B=0x7$ ,  $cin=0 \rightarrow cout=0$ ,  $S=1001$

### FULL ADDER



- ✓ Perform Functional Simulation and Timing Simulation of your design. **Demonstrate this to your TA.**
- ✓ I/O Assignment: Create the XDC file. Nexys A7-50T: Use SW15-SW0 for the inputs, and LED4-LED0 for the outputs.
- ✓ Generate and download the bitstream on the FPGA and test. **Demonstrate this to your TA.**

- Submit (as a .zip file) the five generated files: VHDL code (4 files), VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.

TA signature: \_\_\_\_\_

Date: \_\_\_\_\_